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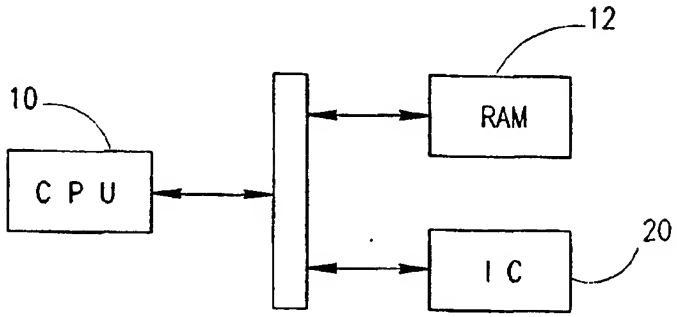
(54) Title: A FLASH MEMORY SYSTEM PROVIDING BOTH BIOS AND USER STORAGE CAPABILITY

(57) Abstract

A flash memory system having a controller (32) and a flash memory device (30) for providing BIOS, operating system and user storage capabilities is disclosed. According to exemplary embodiments of the present invention, flash memory systems can be designed as integrated circuit packages (20) which are pin compatible with conventional ROM BIOS chips (14) so that existing systems can be readily upgraded without extensive modifications.



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A FLASH MEMORY SYSTEM PROVIDING BOTH BIOS AND USER STORAGE CAPABILITY

FIELD AND BACKGROUND OF THE INVENTION

The present invention relates generally to computers and personal digital assistants, and more specifically to an integrated circuit providing both the functionality of BIOS routines and user storage.

Today, every computer and personal digital assistant uses some type of permanent memory to store the software code that provides essential low-level services, commonly called Basic Input/Output Services (BIOS), some type of storage device to provide access to an operating system that provides higher level services, and some type of storage device that allows a user to run application programs and retrieve stored data. For example, a typical configuration in a personal computer is to have the BOIS stored in an integrated circuit located on the motherboard, the operating system stored on a magnetic hard disk drive which has an I/O interface with the motherboard, and to provide volatile memory chips (RAM) into which programs or parts of programs are retrieved from a secondary storage device (e.g., hard disk drive or floppy disk drive) for operation.

While this configuration has proven to be effective, this technology has been, and confines to be, driven by the need for smaller and more powerful computers. The dramatically increasing popularity of laptop and palmtop computers, to be followed in the near future by personal digital assistants, evidences the market pressure for continued technological advances which will allow further miniaturization without sacrificing performance.

Since both magnetic hard disk drives and floppy disk drives are relatively large and somewhat susceptible to mechanical failure, they have become a target for improvement by system designers. Accordingly, one of the many results of this pressure to miniaturize was the development of solid state disk technology (SSD). The basic concept behind SSD

technology is to use integrated circuits, e.g., ROMs, RAMs, and EPROMs, not only as primary system memory, but also as secondary storage so that hard and/or floppy disk drives can be eliminated. Solid state disks have the additional benefits of being smaller, more rugged and consuming less power than conventional magnetic storage.

A newer type of solid state memory, called flash memory, has recently been used in SSD applications. Flash memory components comprise arrays of electrically erasable programmable read-only memory (EEPROM) devices which can be simultaneously erased. Flash memory components have very favorable attributes for use in SSD applications including fast access, low power consumption, high reliability and relatively low cost. Unfortunately, flash devices also have the drawback of being erasable at a block level only. This constraint has conventionally relegated flash memory to the role of read-only memory, which is undesirable in devices purporting to be a substitute for secondary storage devices such as hard disk drives which provide read/write functionality.

Moreover, despite the technical advances in this area, a completely integrated solution has not yet been developed. In particular, there is a need for the various memory devices which store required code, such as the BIOS and the operating system, as well as optional code, such as a user's applications, to be integrated into a single package. This need has not yet been satisfied by today's products.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides solutions to the aforementioned problems by providing, according to exemplary embodiments thereof, the BIOS, an operating system and user storage in a single integrated circuit package. This object is achieved, for example, by providing an application specific integrated circuit (ASIC) controller in conjunction with at least one flash memory device. Thus, according to

exemplary embodiments of the present invention, a flash memory system provides all of the functionality of the BIOS, an operating system and a hard disk, which has previously been found only in separate components.

Further, according to an exemplary embodiment of the present invention, a flash memory system which provides the functionality of BIOS, an operating system, and user storage, is designed as a single integrated circuit package which is pin compatible with existing ROM BIOS chip. This feature provides, among other advantages, for easy and cost-effective retrofitting of existing computers and personal digital assistants by simply replacing a ROM BIOS chip.

Moreover, flash memory systems according to the present invention provide many advantages when incorporated into, for example, portable computer systems and personal digital assistants. For example, such flash memory systems provide faster access times and have lower assembly costs than conventional hard disk drive units, are lower in price than SRAM, and require less space on system boards than other storage solutions.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the present invention will become more apparent upon reading the following detailed description in conjunction with the drawings in which:

Figure 1 is a block diagram of a conventional computer system;

Figure 2 is a block diagram of an exemplary system according to the present invention;

Figure 3 is a block diagram of a flash memory system according to the present invention;

Figure 4 is a memory map of a flash memory device according to an exemplary embodiment;

Figure 5 illustrates windows opened between a flash memory device and system memory according to an exemplary embodiment;

Figure 6 is a block diagram of a controller according to an exemplary embodiment of the present invention;

Figure 7 is a state diagram illustrating operation of a controller according to an exemplary embodiment;

Figure 8 is a flow chart which illustrates interrupt handling according to an exemplary embodiment; and

Figure 9 is a pin diagram of an integrated circuit package according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

As mentioned above, the present invention is applicable to all types of computers and personal digital assistants wherein a ROM BIOS chip or an analogous chip is typically used to store low-level routines. Figure 1 very generally illustrates a layout of some of the typical components of such systems, including g a CPU or microprocessor **10**, a system memory (RAM) **12**, a ROM BIOS chip **14**, and a hard disk drive unit **16**, all of which receive data from, and place data on, a system bus **18**.

According to exemplary embodiments of the present invention, the ROM BIOS chip is replaced by a flash memory system chip which includes the BIOS as well as a solid state disk which is designed to emulate, for example, storage provided by a hard disk unit. Such a system is shown by the block diagram of Figure 2, wherein the flash memory system **20** replaces the ROM BIOS chip **14**. Also omitted from Figure 2 is the hard disk drive unit **16** of Figure 1 since, as will be described in more detail below, the flash memory system can eliminate the need for a hard disk drive unit. Of course, for systems requiring large amounts of secondary storage, hard disk drive unit(s) could be retained or a memory card could be added.

As seen in Figure 3, flash memory systems according to exemplary embodiments of the present invention comprise two basic functional units.

A flash memory device **30** provides the storage capability for the integrated circuit package and a controller **32** provides logic functions which are used to interface the flash memory device **30** with the rest of the system via the system bus. The flash memory device **30** comprises one or more flash memory units.

Figure 4 is a memory map showing how 1 MB of storage in the flash memory device **30** can be used in this exemplary embodiment. The memory is divided into 16 blocks of 64 KB each. The first block (block 0) contains a flash file system which is used to control blocks 2-15 so that they emulate, for example, a hard disk. Block 1 contains the BIOS. Although some of the features of the flash file system contained in block 0 will be discussed by way of the following description of the overall operation of integrated circuit package **20**, the details of this flash file system are beyond the scope of the present disclosure. A suitable flash file system is more fully described in U.S. Patent Application Serial No. 08/027,131, filed on March 8, 1993, and entitled "Flash File System", which is incorporated herein by reference.

The controller **32** provides and controls a window between the system memory **12** and the flash device **30**. Throughout this disclosure the term "window" is used to refer to a memory mapping scheme between the flash memory device **30** and the system memory **12**. When the CPU attempts to access an address in the system memory **12** within the window, a corresponding address in the flash memory device **30** is actually accessed. During start-up, the window can be shifted so as to function either as a window into the BIOS stored in block 1 of the flash memory device **30** or as a window into the flash file system stored in block 0 of the flash memory device.

This feature is diagrammatically illustrated by the dotted lines between the system memory **12** and the flash memory device **30** in Figure 5. In the example illustrated therein, addresses F0000-FFFFF in the system

memory **12** are mapped to addresses in block 1 of the flash memory, and addresses CB0D0-CDFFF in the system memory **12** are mapped to addresses in block 1 of the flash memory, and addresses CB0D0-CDFFF in the system memory are mapped to addresses in block 0 of the flash memory. Of course, it will be appreciated that other groups of addresses in the system memory **12** could be mapped to corresponding addresses in the flash memory **30**.

Figure 6 illustrates an exemplary arrangement for the controller **32**, in block diagram form. A CLKRST circuit **34** receives clocking information from the system bus **18** and provides clock signals and reset signals to the other components of the controller **32**. A CONFIG circuit **36** reads stores the configuration of the flash memory device, e.g., the information indicating where the BIOS and flash file system are stored.

A STATE circuit **38** receives information pertaining to the configuration of the flash memory device **30** and detects access of system memory addresses within the current window. The STATE circuit **38** also identifies and interprets certain attempts to read individual or sequential system memory addresses as instructions to the controller. For example, as described below, accesses to certain addresses are identified as commands to move the window. In response to these control sequences, the STATE circuit **38** switches the window between the BIOS block (block 1) and the flash file system block (block 0). A WINDOW circuit **39** implements the movable window between the flash memory device **32** and system memory **12** based on information and instructions from the CONFIG and STATE circuits. The operation of the flash memory system will now be described.

At power-on, the controller **32** performs a reset and opens a window as a 64 KB window into the BIOS stored in block 1 of the flash memory device **30**. Since there is no reset (RST) pin on BIOS chips or on integrated circuit packages according to exemplary embodiments of the

present invention which are compatible therewith, the controller **32** performs a read from address FFFF0 in the system memory **12**, where the BIOS reset vector is located, which results in an internal reset. Any read from this address will be identified by the STATE circuit **38** as an instruction to the controller **32** to switch the window to block 1 containing the BIOS. During this time, the WINDOW circuit **39** causes external addresses to be mapped directly to the flash addresses in block 1 of the flash memory.

At a point in the BIOS reset routine after the system memory has been initialized, but before the BIOS begins accessing the hard of floppy disk drives, the controller **32** intercepts the disk boot process. In the disclosed embodiment, this operation is carried out by inserting an instruction that causes the system to jump in place. When the controller later detects that the system is jumping in place, the controller switches the window to the flash file system stored in block 0 of the flash memory device **30**, and inserts an instruction that causes the CPU **10** to jump to the beginning of the flash file system. The flash file system installs itself into the system memory **12**, and the system update is completed.

More specifically, when the integrated circuit package **20** is powered up, the CONFIG circuit **36** of controller **32** reads data, for example from addresses FFFC and FFFD of block 0 of the flash memory device **30**, and writes this data into a register. The value stored in the register is the insertion address which is the point in the BIOS reset routine where the controller **32** inserts the jump-in place instruction as above. This step of initially reading the insertion address from the flash memory **30** at the onset of a reset operation is carried out because the desired insertion address can vary among different BIOS versions. Thus, the memory system of the present invention is readily suited to be used with any type of BIOS.

The insertion address is located in segment F000 so that the access to the insertion address will be within the open window and, thus, will be detected by the STATE circuit **38** of controller **32**. Preferably, the area of the system memory **12** that includes the insertion address is not used as cache memory to avoid the possibility that the system would always see the first jump-in-place instruction and hang up.

Figure 7 illustrates the state changes of the controller **32** during a reset operation. As described above, upon receipt of a reset command the controller enters a first state **40** and intercepts the disk boot process, i.e. it outputs the jump-in-place instruction at the proper time in the BIOS routine. After the insertion address stored in the register has been consecutively accessed a number of times, e.g. three times, the controller **32** moves to a second state **42** and inserts the instruction to jump to the beginning of the flash system that is stored in block 0 of the flash memory device **30**. The reading of the register a number of times in succession prevents routine data fetches from accidentally triggering the installation of the flash system stored in the flash memory device since such routine data fetches are not likely to return to the same address three times in succession. Although three consecutive reads from the insertion address are used in this exemplary embodiment to confirm that the processor is performing an instruction fetch from the insertion address rather than a data fetch, those skilled the art will appreciate that two or four or more consecutive reads could be used, depending on the amount of redundancy desired for a particular system.

Once the controller has inserted the instruction to jump to the system install routine, the flash system is installed into the system memory **12**. Thereafter, the CPU returns to the insertion address, i.e., the point where the BIOS reset routine was interrupted, and the controller again changes state. In a third state **44**, the controller block **32** again inserts a jump-in-place instruction at the insertion address. In the same manner as

state **40**, this state ensures that the current reading of the insertion address is intended to indicate that the flash system has been installed by distinguishing ordinary data fetches from an instruction fetch of the insertion address. After the insertion address is accessed three times consecutively, the controller changes to state **46** and outputs the original contents of the BIOS to resume the reset routine where it left off. Thereafter, the controller internally resets itself to the original state **40**, as shown by the arrow leading from state **46** back to state **40**, so that it is at the proper state the next time a reset command is issued.

After the flash file system has installed itself into the system memory, the flash file system switches the window back to the BIOS in block 1 of the flash memory device **30** to complete the boot procedure. Whenever the flash file system starts to run, the window is switched to the portion of the flash memory device **32**, e.g., blocks 2-15, which provides user storage and can be formatted to emulate, for example, a hard drive. The WINDOW circuit **39** maps external addresses to the appropriate block in the flash memory according to the position of the window.

As mentioned above, switching the window to the BIOS can be accomplished by reading from an address containing an internal reset vector, e.g., address FFFF0. In order to switch the window to the flash memory device, the flash system performs three consecutive reads from addresses FFF00, FE0F0, and FD880. This sequence is detected by the STATE circuit **38** which commands the WINDOW circuit to switch the window. Any other reads during this sequence will cancel the sequence which can then be restarted to switch the window to the flash memory. Instruction fetches performed during the sequence will not interfere because they will not read from the system memory area holding the BIOS. Therefore, a chip enable line **37** to the STATE block **38** will not go low, and the controller **32** will not recognize these instruction fetches as data reads.

If an interrupt occurs while switching the window from the BIOS to the flash, the flash system will access the BIOS and the switching sequence will be canceled. Thus, the interrupts should be disabled during the procedure which switches the window from the BIOS to the flash.

In addition to being able to witch the window between the BIOS and the flash memory device **30**, the flash system performs operations for reading the flash memory, positioning the window within the flash memory, erasing the flash memory and writing to the flash memory. When the window is open on the flash, it can be divided into two 32 KB sections. The lower 32 KB of the window can be used as a read space, and the upper 32 KB of the window can be used as a control space. The read space is the actual window into the flash memory. A read from the read space returns the data stored at that location. The control space is used to perform all the operations other than reading from the flash memory.

When the window is open to the flash memory, there can be no accesses to the BIOS. Thus, the flash system will not generate any software interrupts or calls to the BIOS without first switching the window to the BIOS. However, hardware interrupts are frequently generated by the system outside the control of the flash file system, and these interrupts will attempt to directly access the BIOS.

To handle this situation, the flash file system changes the vectors associated with the hardware interrupts when the flash file system switches the window to the flash memory from the BIOS. The original hardware vectors are stored elsewhere and new vectors are substituted therefor which point to flash file system subroutine. This subroutine is illustrated in Figure 8 and described below.

In step **50**, the flash file system checks to see if an erase operation is in progress. If so, the erase operation is suspended at step **52** and the flow proceeds to step **58**. If an erase operation is not in progress, the

progress, the process moves directly to step **58** where the window is switched to the BIOS, e.g., by performing a read of address FFFF0. Since read operations typically take only one bus cycle, as compared to the lengthier erase (and write) operations, they will be completed without the need for special handling prior to servicing the hardware interrupt.

Next, the BIOS code is intercepted during flash programming. In the disclosed embodiment, this interception is carried out by preparing a stack so that an interrupt return instruction (IRET) pointing to this subroutine will be executed following servicing of the hardware interrupt, at step **60**. The hardware interrupt handler in BIOS associated with the interrupt generated by the system is called in step **62**. When the interrupt has been serviced, the window is shifted back to the flash memory device, e.g., by consecutive reads from addresses FFF00, FE0F0, and FD880, and if there was a suspended erase operation, it is resumed at steps **64** and **66**, respectively. Control is then returned to the flash file system stored in system memory **12**.

As mentioned above, exemplary embodiments of the present invention are intended to be pin compatible with existing ROM BIOS chips. Thus, according to one such exemplary embodiment, the integrated circuit **20** can have the pin configuration illustrated in Figure 9 which is that of a standard EPROM, 28-pin DIP chip. In Figure 9, pins A0-A15 are used for address inputs, pins D0-D7 are used for data input and output, pin CE is a chip enable, pin OE is an output enable, pin GND is a ground pin and pin VCC is the power pin.

According to an exemplary embodiment of the present invention, after the flash file system has been installed in the system memory and the remaining BIOS initialization routines have been completed, the flash system can then be instructed to load an operating system which is stored in the user storage area (blocks 2-15) of the flash memory device **30** into system memory. At this point, a computer system or personal digital

assistant incorporating a flash memory system according to the present invention will have very rapidly performed all of the present invention will have very rapidly performed all of the steps necessary to enable a user to access his or her desired applications without accessing a hard disk drive or a floppy disk drive.

The previous exemplary embodiment has been described in terms of a flash memory system which provides 1 MB of storage using a single flash memory device, however those skilled in the art will appreciate that both the size and number of the flash memory devices can be varied. For example, a piggy-back type memory expansion module containing up to three flash memory chips can be added, whereby the disk space can be expanded from 1 MB to 2 or 4 MB. Alternately, custom modules can be designed having up to eight flash memory devices.

While the present invention has been described with respect to the foregoing exemplary embodiments, these embodiments are intended to be in all respects illustrative rather than limitative or restrictive of the present invention. Thus, for example, although the user storage portion of the flash memory device has been described as begin formatted and used in a manner analogous to that of a hard disk drive, those skilled in the art will readily appreciate that the flash system could use this memory to emulate other types of secondary storage, such as an optical drive.

Accordingly, any and all modifications or changes which are within the spirit and scope of the present invention as embodied by the appended claims are intended to be encompassed thereby.

WHAT IS CLAIMED IS:

1. A system, comprising:

system memory means for storing user date;

central processing means for providing control functions of said system;

a system bus for communicating data between said system memory means, said central processing means and a n integrated circuit package;

said integrated circuit package comprising:

flash memory means for storing both BIOS routines and said user data; and

controller means for interfacing said flash memory means and said system bus.

2. The system of claim 1 wherein said controller means provides a window between said flash memory means and said system memory means.

3. The system of claim 1, wherein said flash memory means stores emulation means for allowing a portion of said flash memory means to emulate a hard disk.

4. The system of claim 3 wherein said controller means includes means for intercepting a BIOS boot process to install said emulation means in said system memory.

5. The system of claim 5, wherein said intercepting means includes insertion means for inserting a jump-in-place instruction into one of said BIOS routines in response to a system reset.

6. The system of claim 5, wherein said intercepting means further comprises detecting means for detecting when said jump-in-place instructions has been executed a predetermined number of consecutive times.

7. The system of claim 6, wherein said insertion means causes said central processing means to jump to an address in said flash memory means in response to a result of said detecting means, whereby said emulation means is loaded into said system memory.

8. The system of claim 7, wherein said central processing means completes said one of said BIOS routines after said emulation means has been loaded into said system memory.

9. The system of claim 3, wherein said emulation means replaces original hardware interrupt vectors of said system with vectors pointing to a subroutine in said emulation means.

10. The system of claim 3, wherein said emulation means is controls reading, waiting, and erasing of said portion of said flash memory means.

11. The system of claim 2, wherein said controller means includes address means for detecting accesses to system memory addresses within said window.

12. The system of claim 11, wherein said controller means includes shifting means for shifting said window between different portions of said flash memory device.

13. The system of claim 12, wherein said shifting means shifts said window in response to a detection of an access to at least one predetermined system memory address by said address means.

14. The system of claim 13, wherein said shifting means shifts said window to a portion of said flash memory means which emulates a hard disk drive in response to a detection of predetermined sequence of system memory addresses by said address means.

15. An integrated circuit package, comprising:

flash memory means for storing both BIOS routines and user data;

controller means for controlling access to said flash memory means; and

pin means for providing external connections to said integrated circuit package.

16. The integrated circuit package of claim 15, wherein said pin means comprises a 28-pin DIP configuration.

17. The integrated circuit package of claim 15, wherein: said flash memory means stores emulation means for allowing a portion of said flash memory means to emulate a hard disk.

18. The integrated circuit package of claim 17, wherein said controller means includes means for intercepting a BIOS boot process to install said emulation means in said system memory.

19. The integrated circuit package of claim 18, wherein: said intercepting means includes insertion means for inserting a jump-in-place instruction into one of said BIOS routines in response to a system reset received by said pin means.

20. The integrated circuit package of claim 19, wherein: said intercepting means further comprises detecting means for detecting when said jump-in-place instruction has been executed a predetermined number of consecutive times.

21. A memory system for computers, comprising: a flash memory device that is divided into at least two portions, a first portion of said flash memory device storing low-level service routines for the operation of a computer, and a second portion of said flash memory device being configured to store user-designated information and a controller which operates as and interface between said flash memory device and an associated computer system, said controller including:

windowing means for mapping external addresses of the associated computer system to addresses in a selected portion of said flash memory device, to thereby establish a window to said selected portion of said flash memory device, and

means responsive to memory accesses by the computer system for switching the selected portion of said flash memory device between said first and second portions.

22. The memory system of claim 21, wherein said second portion of the flash memory device includes a first block of memory which stores a flash file management system, and at least one other block of memory which is adapted to store user-designated data.

23. The memory system of claim 22 wherein said switching means is responsive to a command to reset the computer system to cause said windowing means to first establish a window to said first portion of said flash memory device to enable said low-level service routines to be booted therefrom, and wherein said controller includes means for causing said switching means to switch the selected portion to said first block in said second portion of the memory device at a predetermined point in the booting of said low-level service routines, to enable said flash file management system to be accessed during a reset procedure.

24. The memory system of claim 21 wherein said switching means is responsive to an access to a predetermined address by the computer system to switch the selected portion to said first portion, and is responsive to consecutive accesses to a predetermined sequence of plural addresses to switch the selected portion to said second portion of the flash memory device.

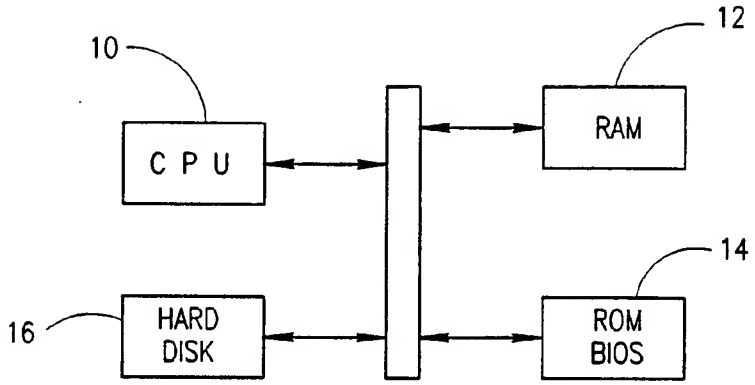

FIG.1

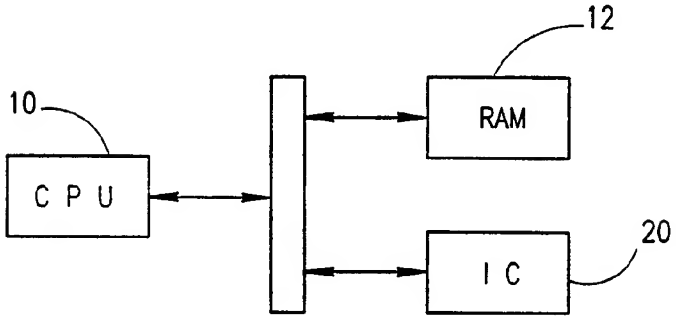

FIG.2

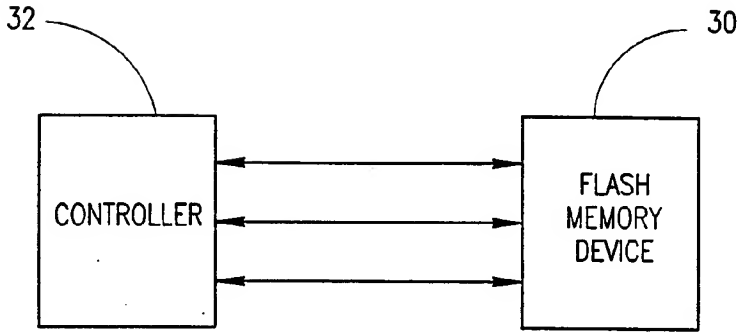

FIG.3

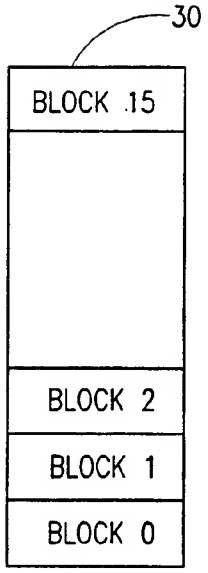

FIG.4

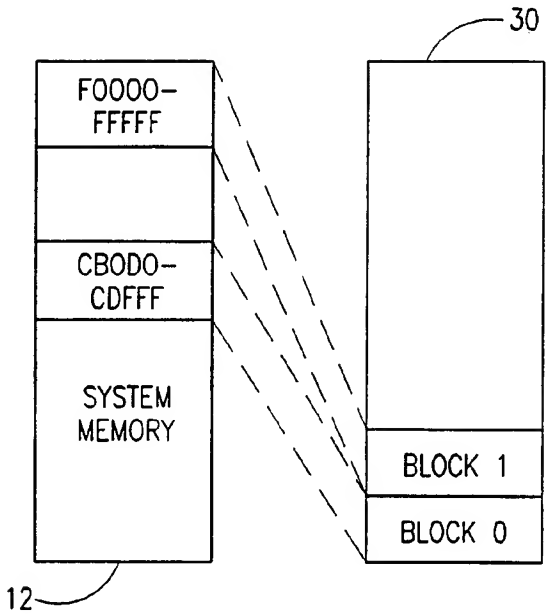

FIG.5

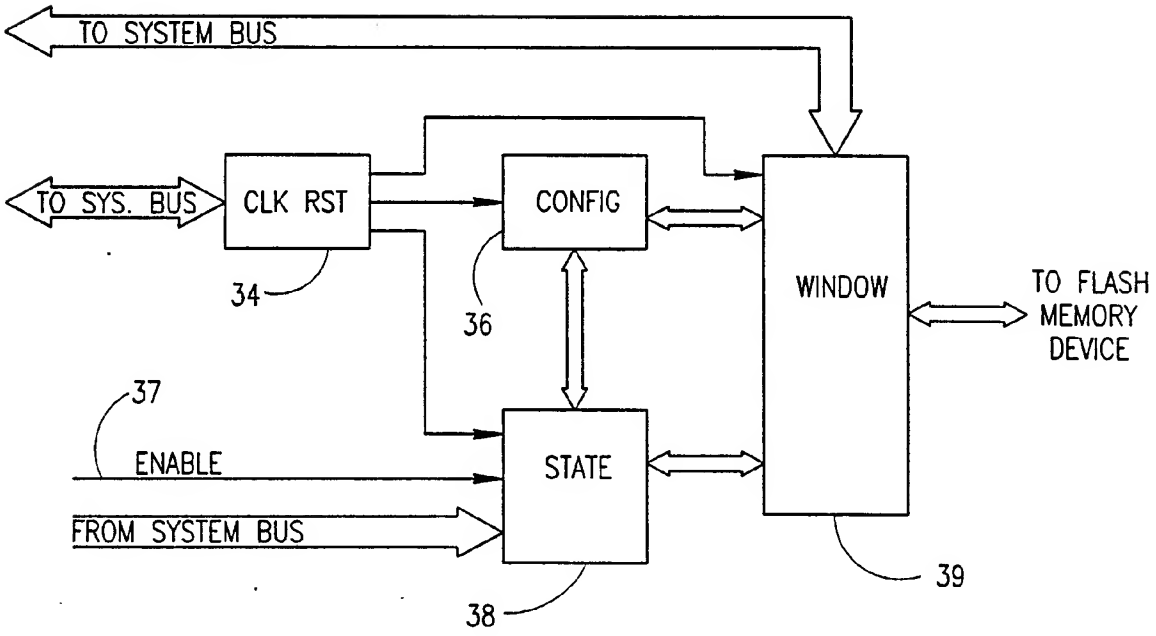

FIG.6

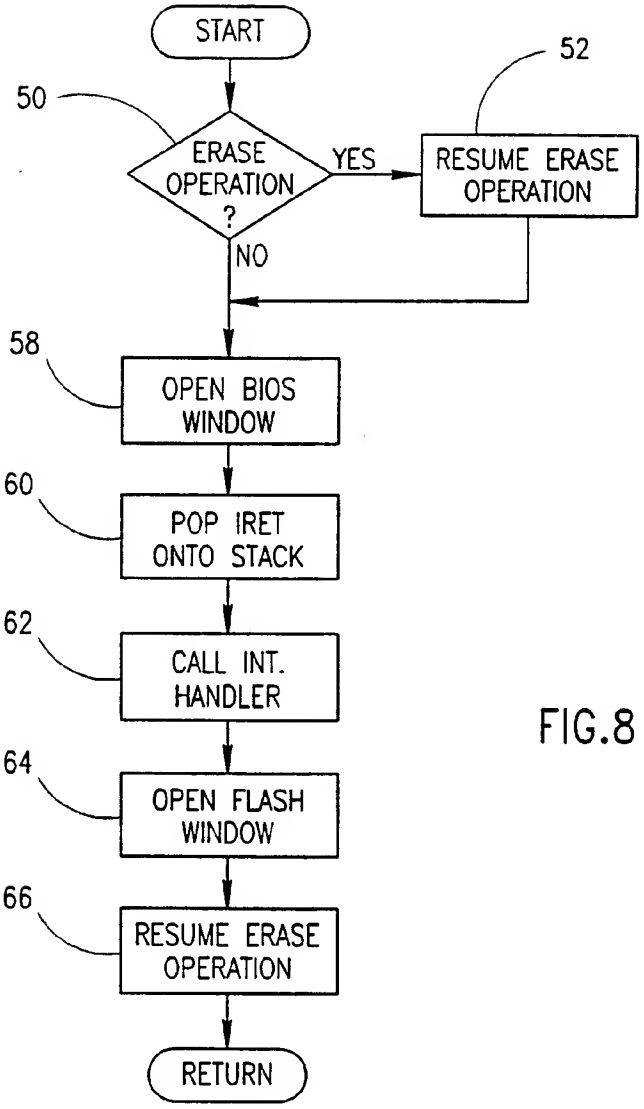
START
50
ERASE OPERATION ?
YES
52
RESUME ERASE OPERATION
NO
58
OPEN BIOS WINDOW
60
POP IRET ONTO STACK
62
CALL INT. HANDLER
64
OPEN FLASH WINDOW
66
RESUME ERASE OPERATION
RETURN

FIG.8

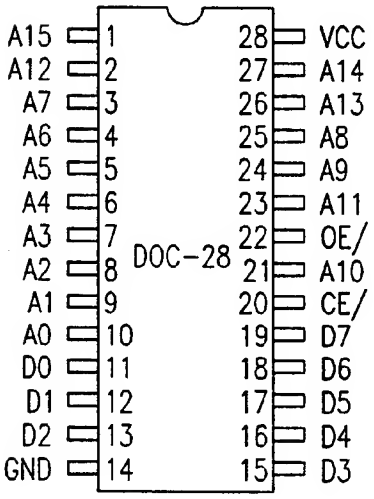
A15 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
D0 11
D1 12
D2 13
GND 14
DOC-28
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 OE/
21 A10
20 CE/
19 D7
18 D6
17 D5
16 D4
15 D3

FIG.9

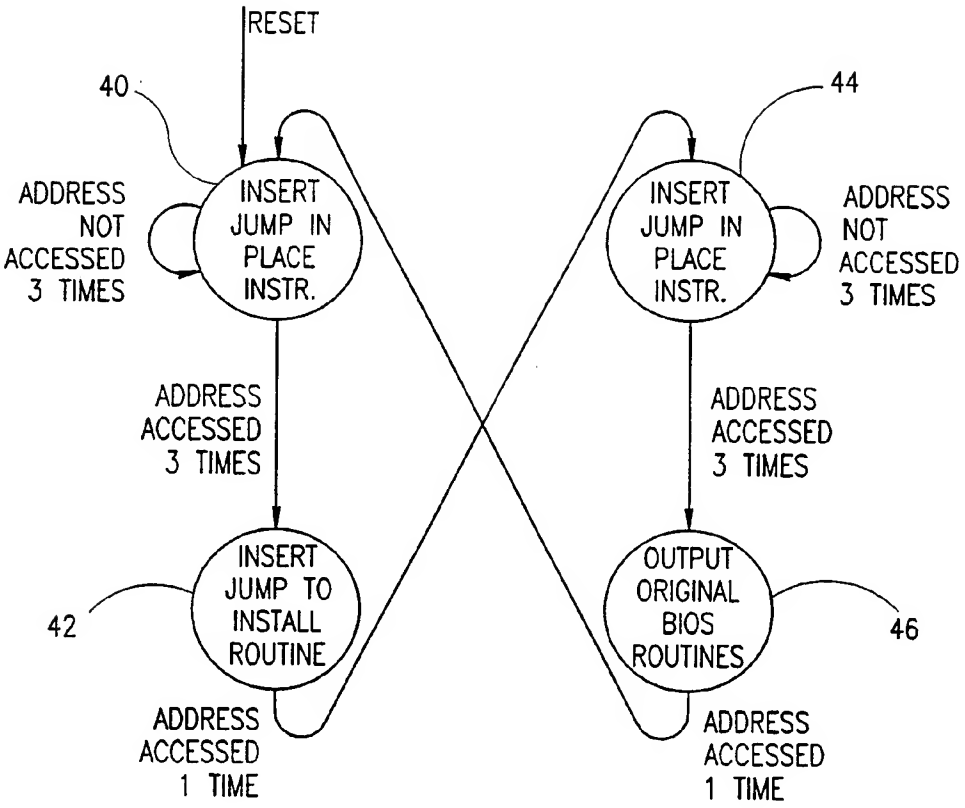
RESET
40
44
ADDRESS NOT ACCESSED 3 TIMES
INSERT JUMP IN PLACE INSTR.
INSERT JUMP IN PLACE INSTR.
ADDRESS NOT ACCESSED 3 TIMES
ADDRESS ACCESSED 3 TIMES
ADDRESS ACCESSED 3 TIMES
INSERT JUMP TO INSTALL ROUTINE
OUTPUT ORIGINAL BIOS ROUTINES
42
46
ADDRESS ACCESSED 1 TIME
ADDRESS ACCESSED 1 TIME

FIG.7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/02576

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G06F 9/06, 12/00, 9/455; G11C 16/00
US CL :395/425, 325, 800, 500; 365/900, 218, 49; 364/431.12
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/425, 325, 800, 500; 365/900, 218, 49; 364/431.12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS,
search terms: BIOS, Boot?, flash memor?, disk emulat?, bus?, control?, (CPU or processor# or micro-processor#)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,218,691 (Tuma et al) 08 June 1993 (08.06.93) Note: (see Fig. 2; col. 4, line 38-col. 10, line 5)	1-4, 8-11, 13-15, 17, 18 and 21
Y,P	US, A, 5,263,003 (Cowles et al) 16 November 1993 (16.11.93) Note: (see Fig. 3; col. 2, line 33-col. 3, line 39)	1-3, 7, 11-15, 17, 21-22 and 24
Y,P	US, A, 5,210,875 (Bealkowski et al) 11 May 1993 (11.05.93) Note: (see Fig. 2; col. 3, lines 6-55)	1-3, 7, 11-15, 17, 21-22 and 24

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 10 MAY 1994	Date of mailing of the international search report JUN 24 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer GOPAL C. RAY Telephone No. (703) 305-9600

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/02576

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,245,572 (Kosonocky et al) 14 September 1993 (14.09.93) Note: (Figures 1-3; col. 2, lines 37-64)	1-3, 7, 11-15, 17, 21-22 and 24
Y,P	US, A, 5,291,584 (Challa et al) 01 March 1994 (01.03.94) Note: (see Fig. 1; col. 2, line 40-col. 3, line 13)	1-4, 8-11, 13-15, 17 18 and 21
Y,P	US, A, 5,293,606 (Sassenrath) 08 March 1994 (08.03.94) Note: (see Fig. 1; col. 2, lines 37-57)	1-3, 7, 11-15, 17, 21-22 and 24
Y,P	US, A, 5,278,759 (Berra et al) 11 January 1994 (11.01.94) Note: (see Fig. 2; col. 4, line 15-col. 5, line 5)	1-3, 7, 11-15, 17, 21-22 and 24
Y	US, A, 5,136,711 (Hugard et al) 04 August 1992 (04.08.92) Note: (see Fig. 1; col. 2, line 35-col. 3, line 28)	1-3, 7, 11-15, 17, 21-22 and 24
Y	US, A, 5,131,089 (Cole) 14 July 1992 (14.07.92) Note: (see Fig. 1; col. 1, lines 5-26	1-4, 8-11, 13-15, 17, 18 and 21
Y	US, A, 5,109,521 (Culley) 28 April 1992 (28.04.92) Note: (see Fig. 1; col. 3, line 40-col. 4, line 12)	1-3, 7, 11-15, 17, 21-22 and 24